



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,039	01/29/2004	Toshiharu Furukawa	ROC920030272US1	4826
30206	7590	07/13/2006		EXAMINER
IBM CORPORATION				CAO, PHAT X
ROCHESTER IP LAW DEPT. 917				
3605 HIGHWAY 52 NORTH				
ROCHESTER, MN 55901-7829				
			ART UNIT	PAPER NUMBER
				2814

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/767,039	FURUKAWA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 09 May 2006.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-5,8-15 and 42-52 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-5,8-15 and 42-52 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 5/9/06.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

1. The Request for Continued Examination filed on 5/9/06 is acknowledged.
2. The cancellation of claims 6-7 and 16-41 in Paper filed on 5/9/06 is acknowledged.

### ***Claim Objections***

3. Claim 1 is objected to because of the following informalities: in claim 1, line 10, a phrase "said vertical passage a vertical dimension" should be changed to "said vertical passage has a vertical dimension". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 42-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Appenzeller et al (US- 2005/0056826) – previous cited).

Regarding claim 42, Appenzeller (Fig. 5n) discloses a vertical Semiconductor device structure, comprising: a substrate 502 defining a substantially horizontal plane; a gate electrode 512 on a right hand side (par. [0040], lines 19-20) projecting vertically from the substrate 502 and including a vertical sidewall; a spacer 503 on a left hand side of a dielectric material (par. [0038], lines 6-7) flanking the

vertical sidewall and spaced horizontally from the vertical sidewall of the right hand side gate electrode 512 to define a vertical passage; a carbon semiconductor nanotube 508 (par. [0038], lines 1-3) positioned in the vertical passage and extending between opposite first and second ends with a substantially vertical orientation; a gate dielectric 511 (par. [0040], lines 13-14) disposed on the vertical sidewall between the semiconductor nanotube 508 and the right hand side gate electrode 512; a source/drain 501 electrically coupled with the first end of the semiconductor nanotube 508; and a source/drain 515 electrically coupled with the second end of the semiconductor nanotube 508.

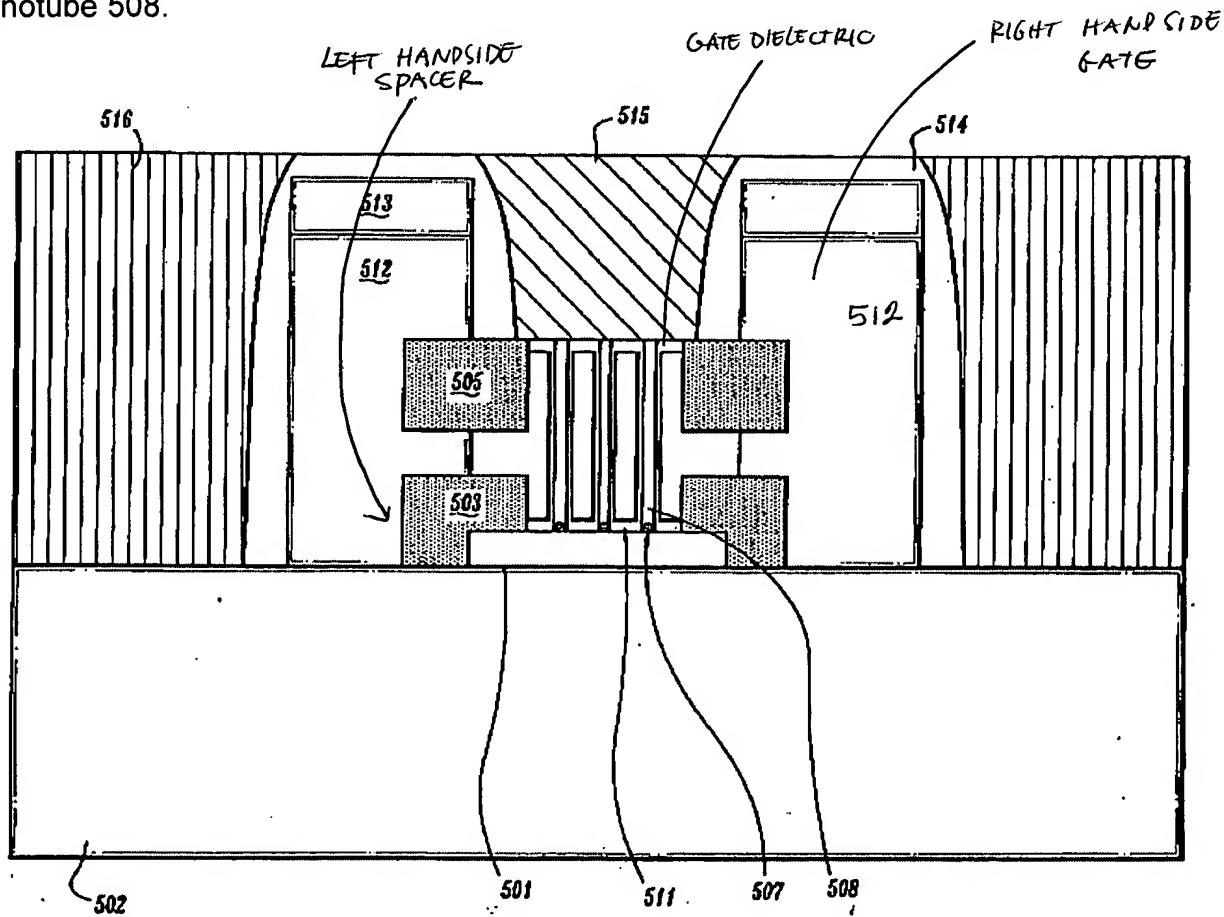


FIG. 5n

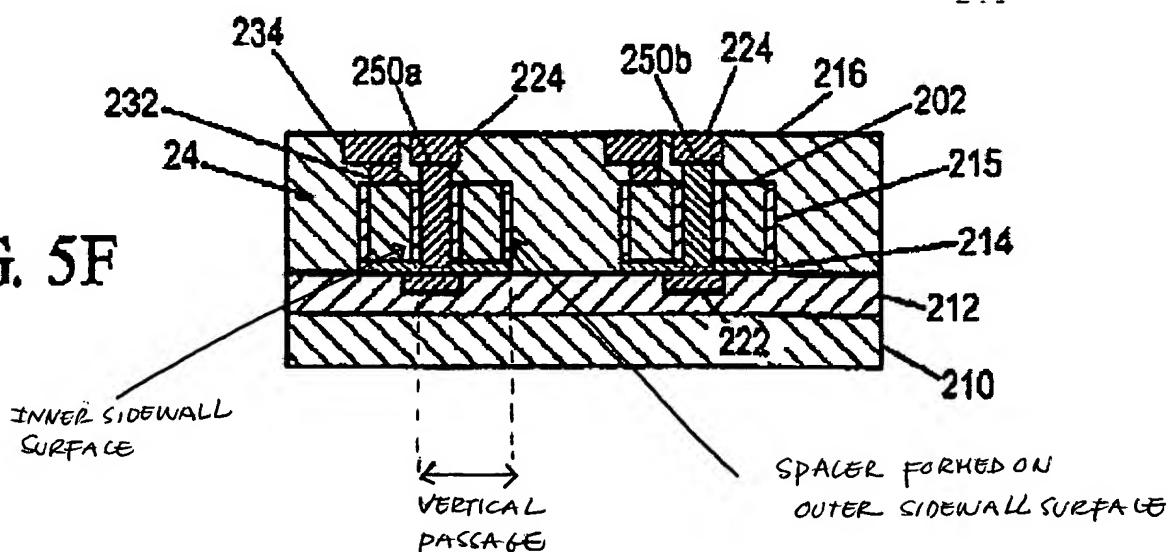
Regarding claim 43-45, Appenzeller (Fig. 5n) also discloses that the top portion of spacer 503 is separated from the substrate 502 by a gap and the spacer 503 is separated from the sidewall by a passage, the nanotube 508 is positioned in the passage, and an insulating material comprising the spacer portion 503 (bottom portion) filling the gap and an insulating layer 511 filling portions of the passage unfilled by the nanotube 508.

6. Claims 1, 5, 8, 12-15, 42-45, 47, and 49-52 rejected under 35 U.S.C. 102(e) as being anticipated by Dubin et al (US. 2005/0167755 – previous cited).

Regarding claims 1, 5, 42 and 47, Dubin (Figs. 5A-5F) discloses a vertical semiconductor device structure, comprising: a substrate 210/212 defining a substantially horizontal plane; a gate electrode 202 projecting vertically from the substrate and including a vertical inner sidewall surface; a semiconducting nanotube 250 of carbon atoms (par. [0045]) extending between opposite first and second ends with a substantially vertical orientation; a spacer 215 of a dielectric material (corresponding to dielectric layer 215 formed on the outer sidewall surface of the ring gate electrode 202) flanking the vertical inner sidewall surface and spaced horizontally from the vertical inner sidewall surface of the ring gate electrode 202 to define a vertical passage having horizontal dimensions appropriate for the synthesis of the semiconducting nanotube 250 (par. [0059]), the semiconducting nanotube 250 positioned in the vertical passage, and the spacer 215 extending relative to the gate electrode 202 such that the vertical passage has a vertical dimension greater than or

equal to a vertical height of the vertical sidewall of the gate electrode 202; a gate dielectric 215 (corresponding to dielectric layer 215 formed on the inner sidewall surface of the ring gate electrode 202) disposed on the vertical inner sidewall surface between the semiconducting nanotube 250 and the gate electrode 202; a source/drain 222 electrically coupled with the first end of the nanotube 250; and a source/drain 224 electrically coupled with the second end of the semiconducting nanotube 250, the gate electrode 202 being positioned between the drain and the source 222 and 250, and the semiconducting nanotube 250 having a length such that the second end of the semiconducting nanotube 202 projects beyond the gate electrode 202 and into the source/drain 224.

FIG. 5F



Regarding claims 8, 12 and 14-15, Dubin (Fig. 5E) further discloses that: the vertical passage has a rectangular cross-sectional profile when viewed in a vertical direction, and a plurality of semiconducting nanotubes 250 are positioned between the gate electrode 202 and the spacer 215, each of the plurality of semiconducting

nanotubes 250 has the first end electrically coupled with the source/drain 222 and the second end electrically coupled with the drain/source 224.

Regarding claims 13, 43-45 and 49-52, Dubin (Fig. 5E) also discloses that the spacer 215 (corresponding to 215 formed on the outer surface of the ring gate electrode 202) is separated from the substrate by a gap and the passage communicates with the gap, and further comprising: an insulating material 214/215 comprising a dielectric material 214 filling the gap and a dielectric layer 215 (corresponding to 215 formed on the inner surface of the ring gate electrode) filling portions of the passage unfilled by the semiconducting tube 250.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 2-4, 9-11, 46 and 48 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Dubin et al (US. 2005/0167755).

Regarding claims 2-3, 9-10, 46, and 48, Dubin (Fig. 5C) further discloses that the source/drain 222/240 is composed of a catalyst material (par. [0059]) effective for synthesizing the nanotube 250 and positioned on the substrate in vertical alignment with the passage.

As to the grounds of rejection under section 103(a), the method of depositing the conductive layers selected from chemical vapor deposition, is an intermediate process step that does not affect the structure of the final device. Therefore, the process limitations (formed by a chemical vapor deposition) recited in a "product by process" claim would not carry patentable weight in a claim drawn to structure because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 4 and 11, Dubin (Fig. 5C) further discloses that the spacer 215 (left 215) is vertically spaced relative to the substrate to define a gap, and the gap is filled by an insulating material 214.

As to the grounds of rejection under section 103(a), the method of depositing the conductive layers selected from chemical vapor deposition or the gap being filled by an insulating material after..., is an intermediate process step that does not affect the structure of the final device. Therefore, the process limitations recited in a "product by process" claim would not carry patentable weight in a claim drawn to structure because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

#### ***Response to Arguments***

9. Regarding the rejections based on Appenzeller, Applicant argues that Appenzeller has been properly disqualified from being used in the ground of rejection against the claims 1-5 and 8-15 by virtual of 35 U.S.C. 103(c) and by Declaration filed under 37 C.F.R. 1.131. The rejection of claims 1-5 and 8-15 based on Appenzeller is

withdrawn. However, the rejection of claims 42-45 based on Appenzeller is still maintained because Appenzeller is still qualified as a prior art under 35 U.S.C. 102(e).

Regarding the rejection of claims 42-45, it appears Applicant argues that in Appenzeller, the gate dielectric 511 is not “disposed on” the sidewall of the gate electrode 512 because the gate dielectric 511 is not directly contact with the sidewall of the gate electrode 512.

This argument is not persuasive because the limitation of having the gate dielectric in direct contact with the sidewall of the gate electrode is not required by the claim language. The term “disposed on” does not necessarily mean that the gate dielectric must be in directly contact with the gate electrode. Therefore, Appenzeller does suggest the invention as claimed because the gate dielectric 511 clearly “disposed on” the sidewall of the gate electrode 512.

The rest of Applicant’s arguments are considered and addressed in view of the new ground of rejections above.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC  
July 7, 2006

*Carmen Mal*  
PHAT X. CAO  
PRIMARY EXAMINER